20V P-Ch Power MOSFET

V_{DS}		-20	V
$R_{DS(on),typ}$	V_{GS}=-10V	2.4	mΩ
$R_{DS(on),typ}$	V_{GS}=-4.5V	2.7	mΩ
$R_{DS(on),typ}$	V_{GS}=-2.5V	3.4	mΩ
I_{D} (Sillicon Limited)		-100	A

Feature
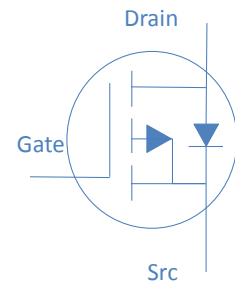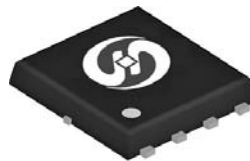◇ High Speed Power Switching, Logic Level
◇ Enhanced Avalanche Ruggedness
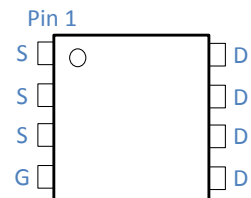◇ 100% UIS Tested, 100% Rg Tested
◇ Lead Free, Halogen Free

Application
◇ Hard Switching and High Speed Circuit
◇ DC/DC in Telecoms and Indutrial

DFN5*6

Part Number	Package	Marking
HTN027P02	DFN5*6	TN027P02

Pin 1

S — D
S — D
S — D
G — D

Absolute Maximum Ratings at T$_j$=25℃ (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	T_C=25℃	-100	A
		T_C=100℃	-73	
Drain to Source Voltage	V_{DS}	-	-20	V
Gate to Source Voltage	V_{GS}	-	±12	V
Pulsed Drain Current	I_{DM}	-	-400	A
Avalanche Energy, Single Pulse	E_{AS}	L=0.1mH, T_C=25℃	500	mJ
Power Dissipation	P_D	T_A=25℃	69	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to150	℃

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	50	℃/W
Thermal Resistance Junction-Case	$R_{\theta JC}$	1.8	℃/W

Electrical Characteristics at T_j=25℃ (unless otherwise specified)

Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=-250μA	-20	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=-250μA	-0.4	-0.60	-1.2	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V, V_{DS}=-16V, T_j=25℃	-	-	-1	μA
		V_{GS}=0V, V_{DS}=-12V, T_j=125℃	-	-	-10	
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±12V, V_{DS}=0V	-	-	±100	nA
Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=-10V, I_D=-20A	-	2.4	2.7	mΩ
		V_{GS}=-4.5V, I_D=-20A	-	2.7	3.2	
		V_{GS}=-2.5V, I_D=-20A	-	3.4	4.1	
Transconductance	g_{fs}	V_{DS}=-5V, I_D=-20A	-	65	-	S
Gate Resistance	R_G	V_{GS}=15mV, V_{DS} =0V, f=1MHz	-	3.0	-	Ω

Dynamic Characteristics

Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=-10V, f=1MHz	-	11116	-	pF
Output Capacitance	C_{oss}		-	1303	-	
Reverse Transfer Capacitance	C_{rss}		-	592	-	
Total Gate Charge	Q_g (10V)	V_{DD}=-10V, I_D=-20A, V_{GS}=-10V	-	202	-	nC
	Q_g (4.5V)		-	87	-	
Gate to Source Charge	Q_{gs}		-	18.0	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	16	-	
Turn on Delay Time	$t_{d(on)}$	V_{DD}=-10V, I_D=-1A, V_{GS}=-10V, R_G=3Ω,	-	20	-	ns
Rise time	t_r		-	55	-	
Turn off Delay Time	$t_{d(off)}$		-	270	-	
Fall Time	t_f		-	100	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_F=-200A	-		-1.2	V
Reverse Recovery Time	t_{rr}	I_F=-20A,dI_F/dt = 100A /μS	-	50	-	nS
Reverse Recovery Charge	Q_{RR}		-	180	-	nC

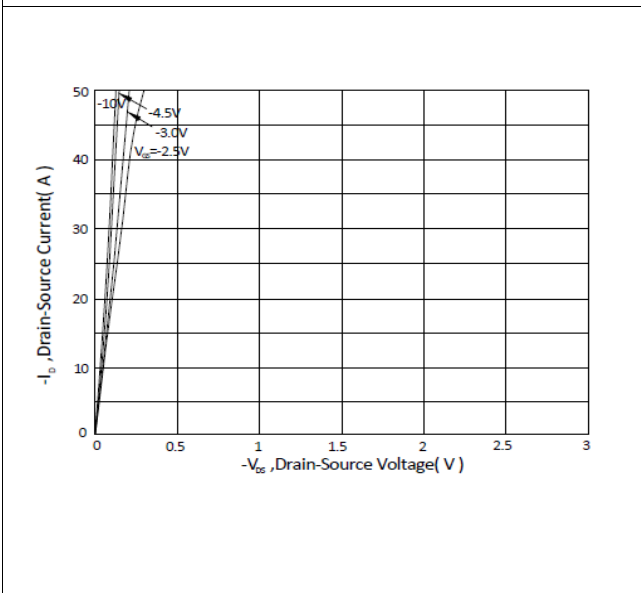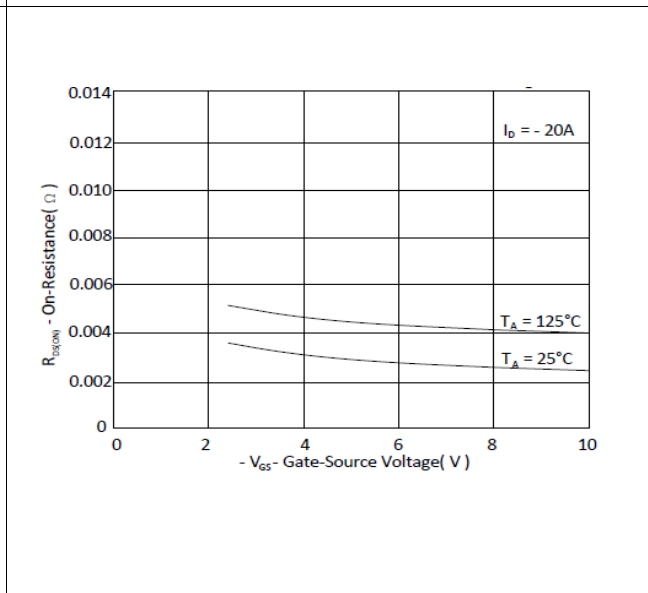| Fig 1. Typical Output Characteristics	Figure 2. On-Resistance vs. Gate-Source Voltage

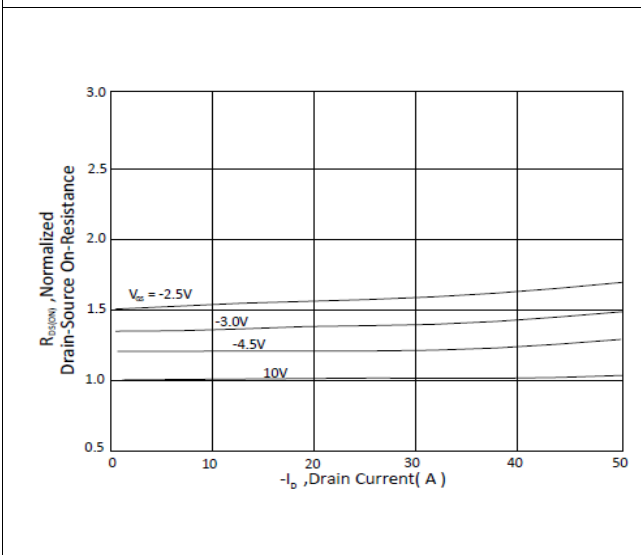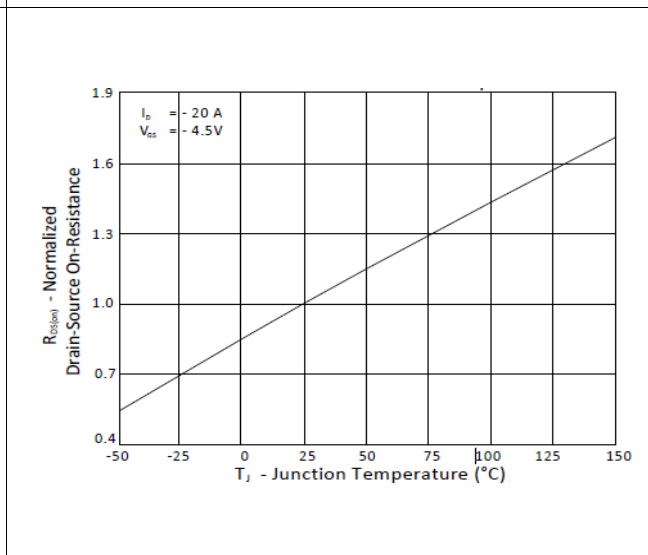| Figure 3. On-Resistance vs. Drain Current and Gate Voltage	Figure 4. Normalized On-Resistance vs. Junction Temperature

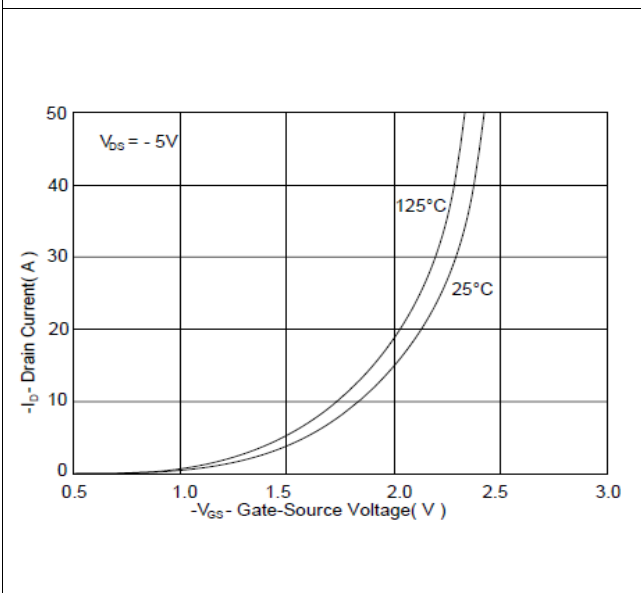
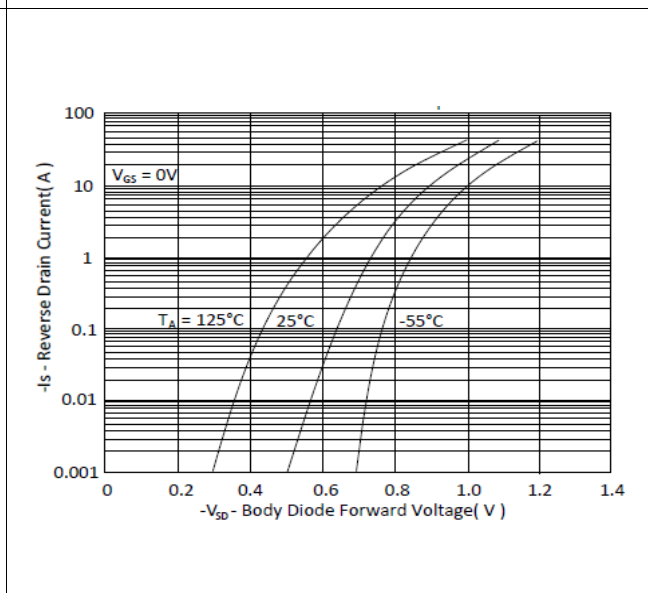| Figure 5. Typical Transfer Characteristics	Figure 6. Typical Source-Drain Diode Forward Voltage

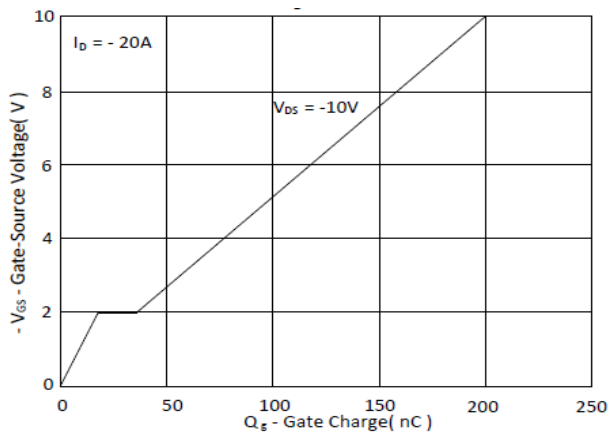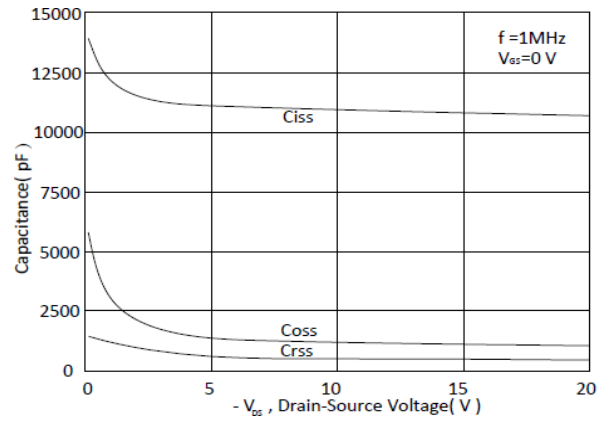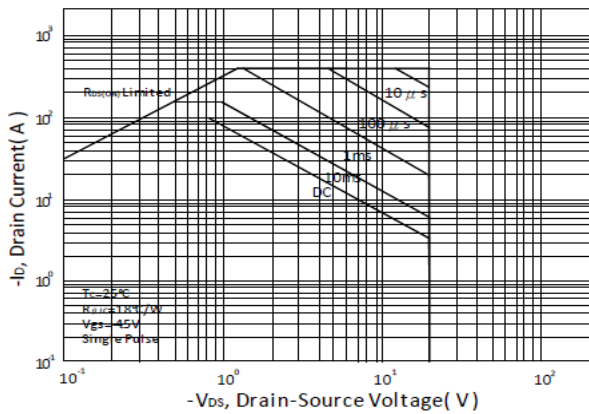| Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage	Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

Figure 9. Maximum Safe Operating Area

Figure 10. Maximun Drain Current vs. Case Temperature
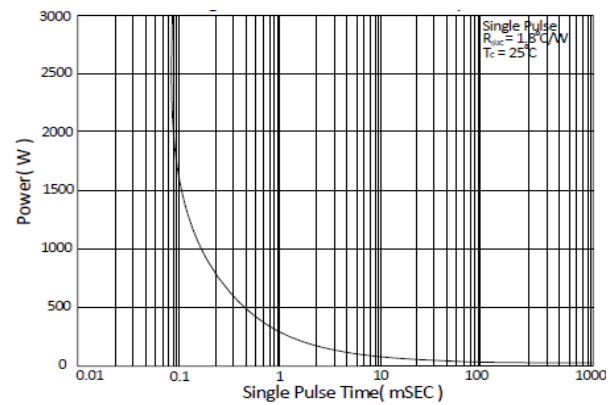
Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient
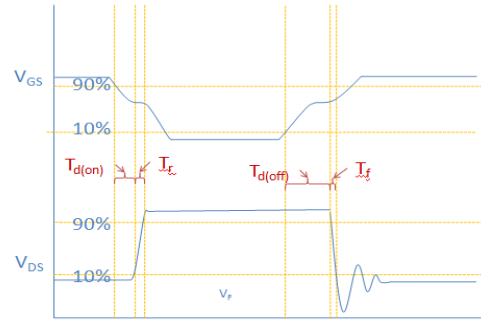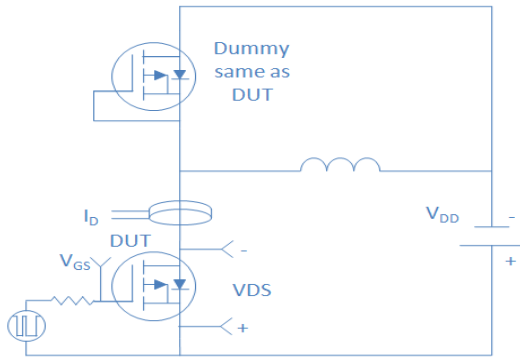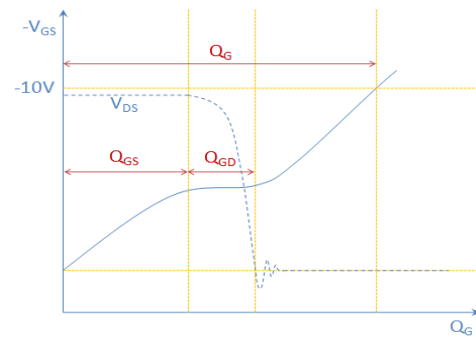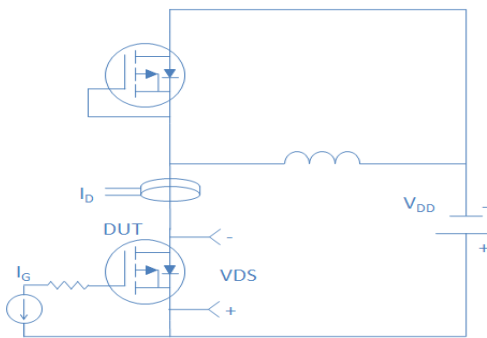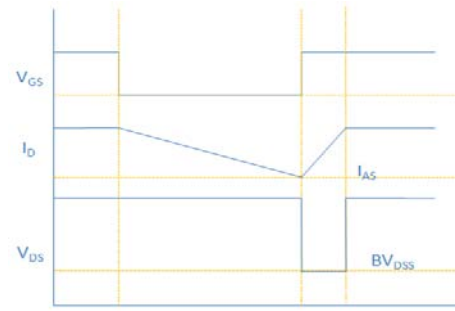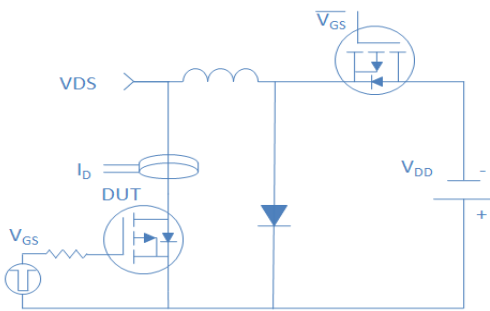
Notes:

1. Duty Cycle, D = $\frac{t1}{t2}$
2. $R_{\theta JC}$ =1.8°C/W
3. T_J - T_C = P * $R_{\theta JC}$ (t)
4. $R_{\theta JC}$ (t)=r(t) * $R_{\theta JC}$
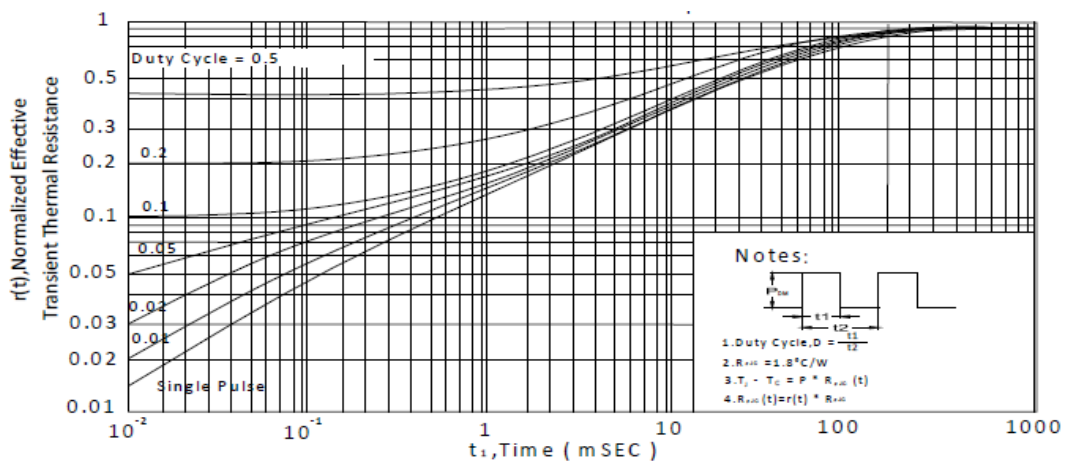
Inductive switching Test

Gate Charge Test

Uclamped Inductive Switching (UIS) Test

Diode Recovery Test
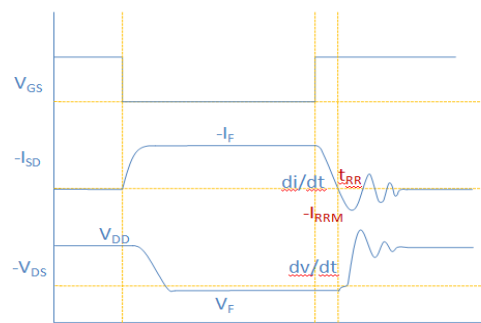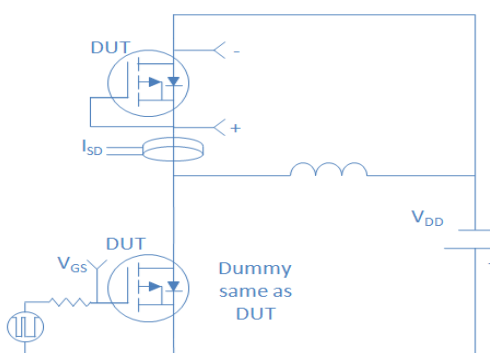
Package Outline

DFN5*6, 8leads

BOTTOM VIEW

TOP VIEW
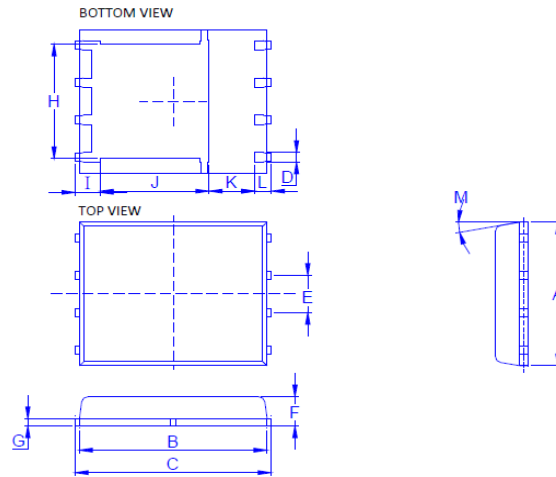
Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K	L	M
Min.	4.80	5.50	5.90	0.3		0.85	0.15	3.67	0.41	3.00	0.94	0.45	0°
Typ.					1.27								
Max.	5.30	5.90	6.15	0.51		1.20	0.30	4.54	0.85	3.92	1.7	0.71	12°